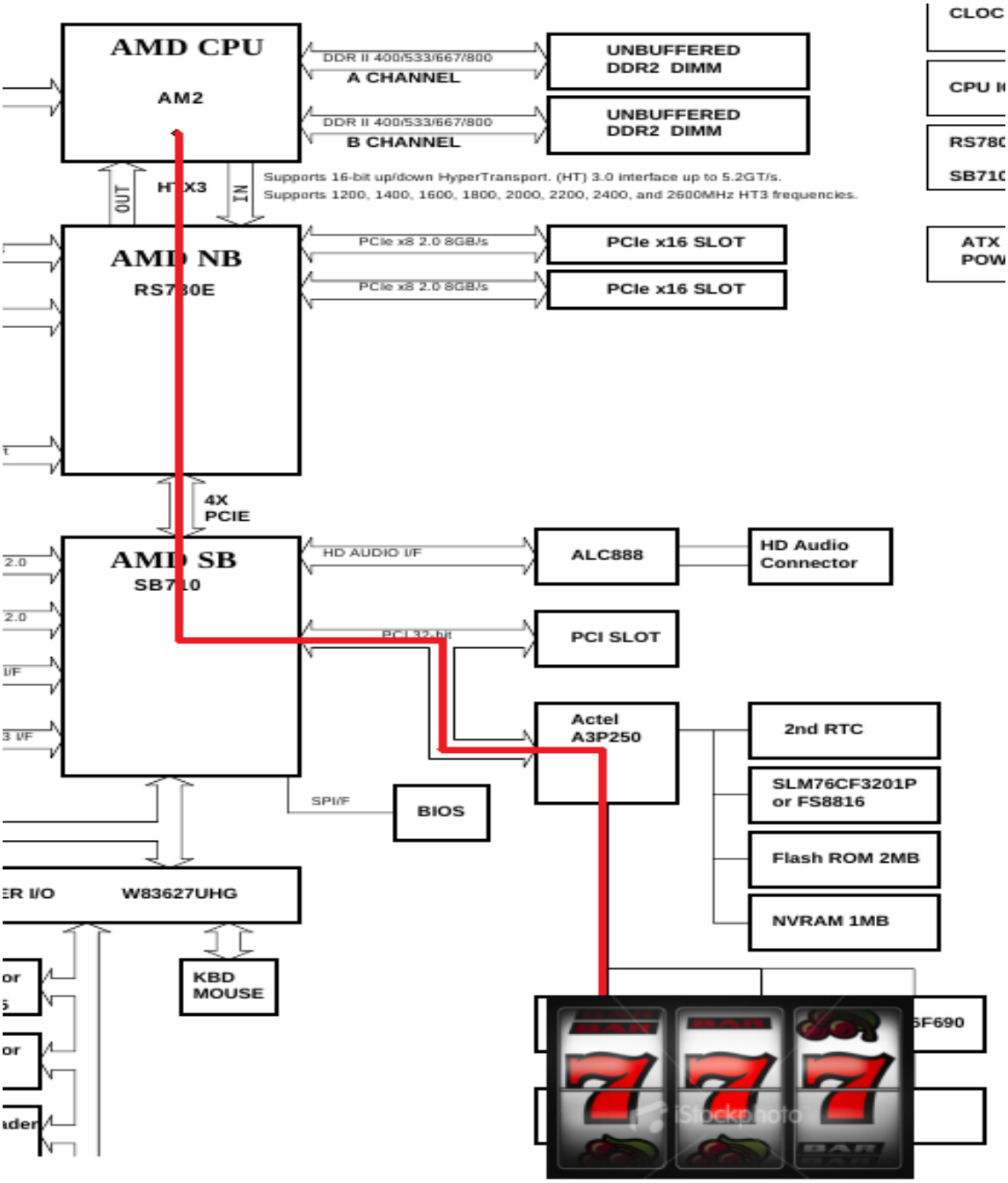
Report on driving a stepper motor via FPGA and interfacing with PCI bus of CPU.

Problem Statement: The task was to interface with the CPU's PCI bus and accept commands given by the CPU and control a 100 step stepper motor attached to the GA5000 board.



Working:

The FPGA uses an IP core for implementing PCI functionality in the FPGA. The logic in the FPGA has to be such that it takes input from the PCI core and then controls the stepper motor as per commands given by the CPU.

The motor unit is at BAR 3 of the PCI slot. So when BAR 3 is selected on the PCI slot the memory io are connected to the motor unit. The " memory_add_i" and the "MEM_DATA_i" and the "MEM_DATA_OUT_i " and the "CE(3)" signals are connected to the motor module.

The Motor supports 3 working modes.

Mode 1: Select speed from 6 available speeds and set the step size of the motor. Start the motor via a start signal. Stop the motor on stop signal. Get the number of rotations of the motor at any time by reading at the specific address.

Mode 2: Select speed from 6 available speeds, set the step size of the motor and number of rotations of the motor. The motor will complete the set number of rotations.

Mode 3: Set the step size and the RMS value as desired and start the motor with a start signal. The operation is same as mode 1 but the speed is customizable.

The logic for driving the motor has the following state machines.

Accepting a command.

When CE = 0 it indicates a command from the pci bus. The logic accepts at the specific adresses commands and sets the necessary registers in the module.

State of the motor

There is a state machine for the state of the motor. The motor according to the mode and the set by the user enters the "laps count" or the "laps control" mode.

According to the speed set by the user the delay between steps is decided. There are 6 set speeds ranging from 110 RPM to 60 RPM. The user according to the mode can set a custom speed also. The delay in that case is derived from the variable set by the user.

The calculation of the delay is as follows for a 100 step motor and a lap size of 100 steps.

Delay for one step = 60*(CLK frequency)/(RPM*100)

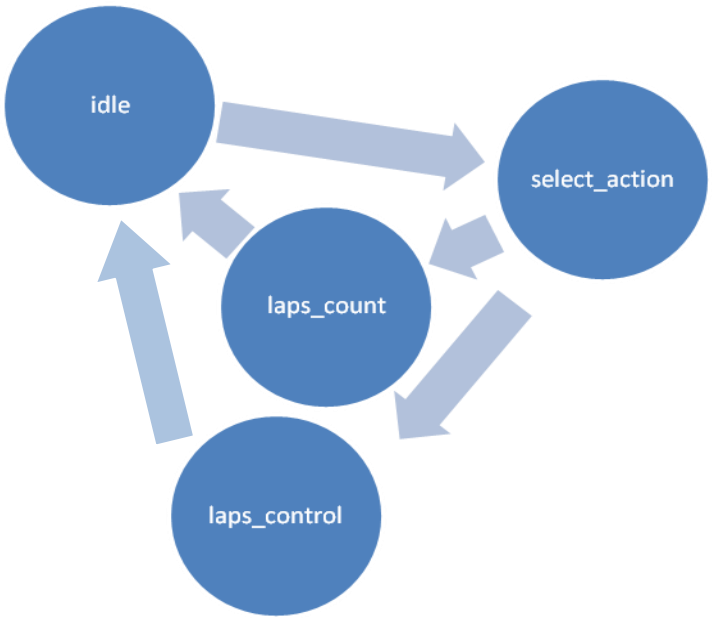
According to the delay and the direction set by the user the motor is given signals as mentioned in the datasheet.

For Forward direction the sequence is

0110->0101->1001->1010

And for reverse the sequence is

0110<-0101<-1001<-1010



I have tested the motor for all functionality of counting laps and the changing in speed and the controlled laps mode.

Miscellaneous learning:

The FPGA by ACTEL has a very good security feature and supports AES encryption. This is important to the customer of the hardware to give him satisfaction regarding protecting his software from being pirated.

References:

Datasheet of the motor RM12_CON2(Used for knowing the signals to give for forward and reverse motion)

FPGA code provided by AEWIN(used for studying the PCI IP core behavior)